UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,084	10/12/2001	G. Michael Uhler	MIPS:0140.00US	1919

23669 7590 11/17/2006

HUFFMAN LAW GROUP, P.C.
1900 MESA AVE.
COLORADO SPRINGS, CO 80906

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,084	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *32-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,3,10,23,28,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (patent No. 5,115,506) in view of Sato (patent No. 5,459,682).

1. Cohen taught the invention substantially as claimed including a data processing ("DP") system comprising (As per claim 1):

2. A plurality of register sets (Normal register set and alternate register set)(e.g, see figs 1a, 1b); an interrupt vector generator for generating an exception vector associating with the interrupt handler, when the processing system receives and interrupt (e.g., see fig. 2 and col. 3, line 64-col. 4, line 8); mapping logic coupled to both of the register sets and the interrupt vector generator for selecting on of said plurality of register sets to be used by the interrupt handler (e.g., see col. 3, lines 13-45) wherein the mapping logic is programmably provided with a correlation between the exception vector and the selected on of the plurality of register sets (e.g., see col. 3, lines 13-45). As to the limitation of the register sets being shadow register sets the only requirement of the registers sets to be shadow register sets is that they are the same in size. Each of the

registers sets of Cohen are the same as the other register set and therefore each provides a separate shadow register set. Together they provide for plural shadow register sets. Cohen did not expressly detail the shadow mapping logic comprises a plurality of entries, each of which is programmable to associate exception vectors with a at least one of the plurality of shadow register sets. However Sato taught storing in a data memory register select data that is used to by a register set selector to select which register set would be used when a particular interrupt occurred (e.g., see col. 3, lines 2-32), and an interrupt memory (63) to store the content of the select data memory (44) where the data used to select the register set for a particular interrupt can be changed using register set select change enable data stored in program memory along with vector data(51) (e.g., see col. 4, lines 4-37). As to the plurality of entries it would have been obvious to one of ordinary skill that since Sato taught plurality of interrupts (e.g., see fig. 3 and col. 4, lines 20-43) and storing data for determining which register set (e.g., see fig. 1 and col. 3, lines 5-37) was to be accessed during the interrupts then the Sato system would have contained plural entries for the plural interrupts (e.g., see fig. 3). This register set selector along with the select data memory and interrupt memory and program memory that stored vector data[that relates to a leading address of the an interrupt service routine see col. 3, lines 17-26], register set select change data and register select change enable data that is selectively accessed for altering which register set is accessed during any particular interrupt of plural interrupts in the Sato system provides for the claimed mapping logic and interrupt generator.

3. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Cohen and Sato. Both references were directed to the problems of efficiently switching register sets upon occurrence of an interrupt (e.g., see col. 1, line 55-col. 2, line 25 of Sato). One of ordinary skill would have been motivated to incorporate the Sato teachings of storing data for changing the register set in rewritable memory at least to provide for a more flexible system facilitating real-time interrupt processing (e.g., see col. 2, lines 6-25).

4. As the limitations of claim 28, 31, where the features discussed above are claimed as program code for providing the elements claimed since Cohen system comprised processor on a semiconductor chip that provided for interrupts it would have been anticipated that the features would have been programmed for controlling the elements as discussed above. The use of hardware or software for the particular portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

5. As per claim 2, Cohen taught each of the plurality of shadow register sets compromise a plurality of duplicate register sets comprise a plurality of registers that duplicate registers of a general purpose (GPR set) (e.g., see col. 3, lines 7-28).

6. As per claim 3, Cohen taught the correlation comprises a maps an exception vector to one of said plurality of shadow register sets (e.g., see col. 3, lines 29-63).

7. As per claim 10,11,12 Cohen taught a status register, for storing data corresponding to a current shadow set, and a previous shadow set (e.g., see CSC register and CSC' register (e.g., see fig. 1C). Sato taught storing data comprising a

program status word for the plurality interrupts as to which register set was to be used for the particular interrupt (e.g. see col. 3, lines 8-12). Therefore one of ordinary skill would have been motivated store in the program status register data for a current register set and a shadow register set indicating the register set to be accessed for each interrupt. Clearly one of ordinary skill would have recognized that in at least one implementation of the Cohen and Sato teachings the data for the current set and shadow set would have been stored in specific locations wherein when the a change or register set would have been performed the change in location of the data would have occurred. This would have facilitated the system in accessing the data for the current or shadow data at the location of each would have been established.

8. As per claim 23, Cohen taught a microprocessor (semiconductor chip 12 with CPU 14) having a first register set (normal register set) for use by non-interrupt instructions, and a second (Normal register set) and third register sets(alternate register) for use by interrupt service routines the microprocessor comprising: a vector generator, for generating exception vectors corresponding to the interrupt service routines; and mapping logic, coupled to said vector generator, for selecting between the second and third register sets for use by the interrupt service routines based on a value of said exception vectors interrupt (e.g., see fig. 2 and col. 3, line 64-col. 4, line 8)[Cohen taught in the body of the claim and plurality shadow registers however does not reference first register set and does not require the first register set and therefore the use of a first register set is given no weight.

Claims 1,2,3,4,7,8,9,14,15,20,22,23,26,27,28,31 rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin in view of Sato.

9. Maupin taught invention substantially as claimed comprising a data processing ("DP") system comprising: (As per claims 1,2,14,20,22,23): a plurality of shadow register sets with addressable registers (46a,46b,46c,46d, 46e,46f,46g) a least one for default task and plurality of register sets each shadow register set dedicated to a different interrupt source (e.g., see col. 2, lines 56-64); interrupt vector generator (e.g., see col. 5, lines 35-44) and shadow set mapping logic coupled to register sets and interrupt generator (e.g., see col. 6, lines 16-32)[task-Ids assigned to interrupt sources and execution core correlates task-ID to interrupt source and using interrupt task-ID to select register set (46a-46H).

10. Maupin did not expressly detail the shadow mapping logic comprises a plurality of entries, each of which is programmable to associate exception vectors with a at least one of the plurality of shadow register sets. However Sato taught storing in a data memory register select data that is used to by a register set selector to select which register set would be used when a particular interrupt occurred (e.g., see col. 3, lines 2-32), and an interrupt memory (63) to store the content of the select data memory (44) where the data used to select the register set for a particular interrupt can be changed using register set select change enable data stored in program memory along with vector data(51) (e.g., see col. 4, lines 4-37). As to the plurality of entries it would have been obvious to one of ordinary skill that since Sato taught plurality of interrupts (e.g., see fig. 3 and col. 4, lines 20-43) and storing data for determining which register set

(e.g., see fig. 1 and col. 3, lines 5-37) was to be accessed during the interrupts then the Sato system would have contained plural entries for the plural interrupts (e.g., see fig. 3). This register set selector along with the select data memory and interrupt memory and program memory that stored vector data[that relates to a leading address of the an interrupt service routine see col. 3, lines 17-26], register set select change data and register select change enable data that is selectively accessed for altering which register set is accessed during any particular interrupt of plural interrupts in the Sato system provides for the claimed mapping logic and interrupt generator. Further as to the type of memory (i.e. registers that stored claimed data) One of ordinary skill would have been motivated at the time of the claimed invention to utilize high speed memory (i.e., registers) to facilitate the real-time interrupt processing and register set changes as taught by Sato (e.g., see 2, lines 7-27) and take advantage of the reduced cost of memory at the time of claimed invention versus at the time Sato patent was filed.

11. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Maupin and Sato. Both references were directed to the problems of efficiently switching register sets upon occurrence of an interrupt (e.g., see col. 1, line 55-col. 2, line 25 of Sato). One of ordinary skill would have been motivated to incorporate the Sato teachings of storing data for changing the register set in rewritable memory at least to provide for a more flexible system facilitating real-time interrupt processing (e.g., see col. 2, lines 6-25 of Sato).

12. As the limitations of claim 28, 31, where the features discussed above are claimed as program code for providing the elements claimed since Maupin system comprised processor on a semiconductor chip that provided for interrupts it would have been anticipated that the features would have been programmed for controlling the elements as discussed above. The use of hardware or software for the particular portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

13. As per claim 3, Maupin taught the correlation comprises a map register that maps the exception vector to a selected one of the plurality of register sets (task-id register) e.g., see col.5, lines 35-55 and col. 6, lines 16-28)[value in the task register used to map the exception vector or interrupt source to register set];

14. As per claim 4 Maupin taught the interrupt vector generator selects a particular one of a plurality of interrupt routines to be used to handle the interrupt (e.g., see col. 5, lines 34-44);

15. As per claim 7, 14 Maupin taught a mapping logic comprising a plurality of programmable fields, each corresponding to one of a plurality of exception vectors, each of the plurality of fields containing data referencing one of the plurality of shadow register sets (e.g., see col. 5, lines 34-55). Maupin did not expressly detail the shadow mapping logic comprises a plurality of entries, each of which is programmable to associate exception vectors with at least one of the plurality of shadow register sets. However Sato taught storing in a data memory register select data that is used to by a

register set selector to select which register set would be used when a particular interrupt occurred (e.g., see col. 3, lines 2-32), and an interrupt memory (63) to store the content of the select data memory (44) where the data used to select the register set for a particular interrupt can be changed using register set select change enable data stored in program memory along with vector data(51) (e.g., see col. 4, lines 4-37). As to the plurality of entries it would have been obvious to one of ordinary skill that since Sato taught plurality of interrupts (e.g., see fig. 3 and col. 4, lines 20-43) and storing data for determining which register set (e.g., see fig. 1 and col. 3, lines 5-37) was to be accessed during the interrupts then the Sato system would have contained plural entries for the plural interrupts (e.g., see fig. 3). This register set selector along with the select data memory and interrupt memory and program memory that stored vector data[that relates to a leading address of the an interrupt service routine see col. 3, lines 17-26], register set select change data and register select change enable data that is selectively accessed for altering which register set is accessed during any particular interrupt of plural interrupts in the Sato system provides for the claimed mapping logic and interrupt generator. Further as to the type of memory i.e. registers that stored claimed data) One of ordinary skill would have been motivated at the time of the claimed invention to utilize high speed memory (i.e., registers) to facilitate the real-time interrupt processing and register set changes as taught by Sato (e.g., see 2, lines 7-27) and take advantage of the reduced cost of memory at the time of claimed invention versus at the time Sato patent was filed.

16. As to the off core and on core interrupts (claim 15), Maupin taught external source register set (46G) for external interrupts and A/D register set for internal A/D interrupt (e.g., see fig. 2 and col. 3, lines 37-67).

17. As per claim 8, Maupin taught eight different register sets and therefore since it would require four bits to select between eight register sets (e.g., see fig. 2)(one for each interrupt source) then one of ordinary skill would have been motivated to employ four bits for the programmable fields.

18. As per claim 9, 20, 22 , Maupin taught the data in each of the plurality of fields corresponds to one of plurality of shadow register sets (e.g., see col. 5, line 34-col. 6, line 2).

19. As per claim 26, 27, Maupin taught upon receipt of an interrupt, determining which one of a plurality of exception routines should be executed (e.g., see col. 4, lines 1-10); and based on the received interrupt, selecting one of a plurality of shadow register sets to be utilized by the one of the plurality of exception routines wherein the step of selecting utilizes programmable registers that contain data indicating which one of the plurality of shadow register sets is to be used for its register (e.g., see col. 4, lines 11-36). Maupin also taught that each of the programmable registers corresponds to one of the exception routines (e.g., see col. 6, lines 16-29).

Claim Rejections - 35 USC § 103

Claims 10,11,12,13,24,25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin in view of Sato (patent No. 5,459,682) .

20. Maupin taught the invention substantially as claimed including a data processing ("DP") system comprising: a plurality of shadow register sets with addressable registers (46a,46b,46c,46d, 46e,46f,46g) a least one for default task and plurality of register sets each shadow register set dedicated to a different interrupt source (e.g., see col. 2, lines 56-64); interrupt vector generator (e.g., see col. 5, lines 35-44) and shadow set mapping logic coupled to register sets and interrupt generator (e.g., see col. 6, lines 16-32)[task-Ids assigned to interrupt sources and execution core correlates task-ID to interrupt source and using interrupt task-ID to select register set (46a-46H).

21. As per claim 24,25 Maupin taught a status register)(storing task-Id) (e.g., see col. 6, lines 16-28) Maupin did not specifically detail the data corresponding to a current shadow set and a previous shadow set (or corresponding to first and second exception vector or data referencing either the second register set or the third register set).

22. Sato taught storing data comprising a program status word for the plurality interrupts as to which register set was to be used for the particular interrupt (e.g. see col. 3, lines 8-12). Therefore one of ordinary skill would have been motivated store in the program status register data for a current register set and a shadow register set indicating the register set to be accessed for each interrupt. One of ordinary skill would have motivated to provide that in at least one implementation of the Maupin and Sato

teachings the data for the current set and shadow set would have been stored in specific high speed locations wherein when the a change or register set would have been performed the change in location of the data would have occurred. This would have facilitated the system in accessing the data for the current or shadow data at the location of each would have been established.

23. As per claim 10,11, Maupin taught a status register)(storing task-Id) (e.g., see col. 6, lines 16-28). Maupin also taught providing separate registers sets to eliminate the need to store data of a current task for speeding processing. Maupin did not specifically detail the status data registers corresponding to a current shadow set and a previous shadow set (or corresponding to first and second exception vector or data referencing either the second register set or the third register set). Sato taught storing data comprising a program status word for the plurality interrupts as to which register set was to be used for the particular interrupt (e.g. see col. 3, lines 8-12). Therefore one of ordinary skill would have been motivated store in data the status registers data for a current register set and a shadow register set indicating the register set to be accessed for each interrupt. This would have facilitated the access to the status data for the particular task. One of ordinary skill would have recognized that in at least one implementation of the Maupin and Sato teachings the data for the current set and shadow set would have been stored in specific locations wherein when a change of register set would have been performed the change in location of the data would have occurred. This would have facilitated the system in accessing the data for the current or shadow data at the location of each would have been established.

24. As per claim 12,13 The saving of the status of registers upon occurrence of an interrupt and restoring the context are the interrupt was serviced was well known in the art at the time of the claimed invention.

25. Claims 5,6,17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin and Sato as applied to claims 1-4,14,15 above, and further in view of M. Morris Mano (book entitled Computer system Architecture) hereafter referred to as Mano.

26. As per claim 5,18 Mano taught the selected particular one of a particular of the interrupt routines is located in a memory at the corresponding exception vector (e.g., see pages 440-441 under Software routines section).

27. As per claim 6,17, Mano taught the interrupt vector generator selected a particular one of a plurality of interrupt routines to be used to handle the interrupt based on the priority level of the interrupt (e.g., see pages 437-441).

28. As per claim 19 Maupin taught the interrupt vector generator selects a particular one of a plurality of interrupt routines to be used to handle the interrupt (e.g., see col. 5, lines 34-44).

29. As the limitations of claim 28, 30, where the features discussed above are claimed as program code for providing the elements claimed since Maupin system comprised processor on a semiconductor chip that provided for interrupts it would have been anticipated that the features would have been programmed for controlling the elements as discussed above. The use of hardware or software for the particular

portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

30. It would have been obvious one of ordinary skill in the DP art to combine the teachings of Maupin and Mano. Maupin taught system where interrupt were generated and serviced using plural register sets (e.g., see col. 5, lines 35-44) but did not specify the circuitry for controlling the access to interrupt handling routines. Mano taught the conventional means and method for implementing the handling of interrupts in a DP system. Therefore one of ordinary skill in the DP art would have been motivated incorporate the teachings of Mano at least to implement effectively Mano teachings.

Allowable Subject Matter

Claims 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER